#12 Appeal Brief 10/21/03 ajg

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Robert A. Street, Ping Mei, Jeffrey T. Rahn

Assignee: Xerox Corporation

Title: LOW DATA LINE CAPACITANCE IMAGE SENSOR ARRAY USING AIR-GAP METAL CROSSOVER

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Examiner: P. E. Brock II Art Unit: 2815

Atty. Dkt. No.: A0682 (XC-004)

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APPEAL BRIEF

Sir:

This Appeal Brief, filed in triplicate, is in support of the Notice of Appeal dated August 1, 2003.

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INDEX

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Xerox Corporation, pursuant to the Assignment recorded in the U.S. Patent and Trademark Office on July 2, 2001 on Reel 011992, Frame 0527.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-10 and 21-30 are pending. Claims 23 and 24 stand withdrawn by the Examiner. Claims 1-10, 21 and 24-30 stand rejected.

In the present paper, rejected Clams 1-10, 21 and 24-30 are appealed, and reinstatement of Claims 22 and 23 is requested.

Pending Claims 1-10 and 21-30 are listed in Appendix A.

IV. STATUS OF AMENDMENTS

Appellant filed a Response to the Final Office Action on June 18, 2003. This Response included an amendment to Claim 27, which was considered and entered by the Examiner.

V. SUMMARY OF THE INVENTION

The present invention is directed to an integrated circuit (e.g., an image sensor) including an array of pixel circuits arranged in rows and columns. For example, Applicants' Fig. 1 (reproduced below for reference) shows a simplified image sensor 100 including an array of pixels 110, each pixel 110 including a sensor 112, an optional storage capacitor 114, and a thin film transistor (TFT) (access transistor) 116. An external scanning control

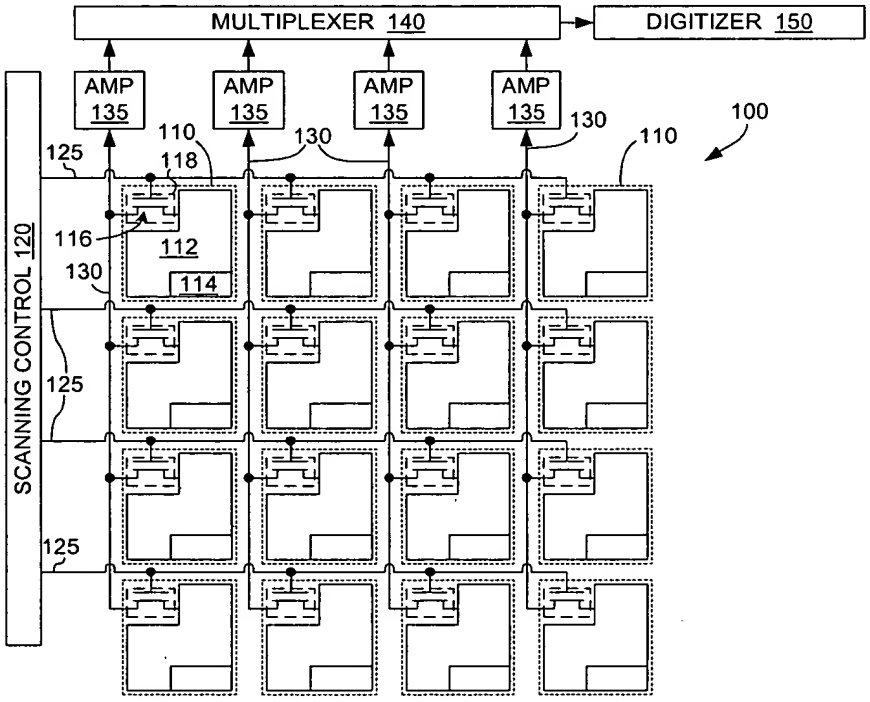

FIG. 1

circuit 120 turns on the TFTs 116 one row at a time via a series of parallel gate (first) lines 125. As each row of TFTs 116 is turned on, an image charge is transferred from the corresponding sensors 112 to a series of parallel data (second) lines 130, which are respectively connected to external readout amplifiers 135. The resulting amplified signal for each row is multiplexed by a parallel-to-serial converter or multiplexer 140, and then transmitted to an analog-to-digital converter or digitizer 150.

Applicants' Fig. 2 (reproduced below for reference) shows a pixel circuit 110 of image sensor 100 in additional detail, and indicates a cross-over capacitance C_{DG} between gate line 125 and data line 130 at each crossover location 210 (i.e., where data line 130 crosses over gate line 125).

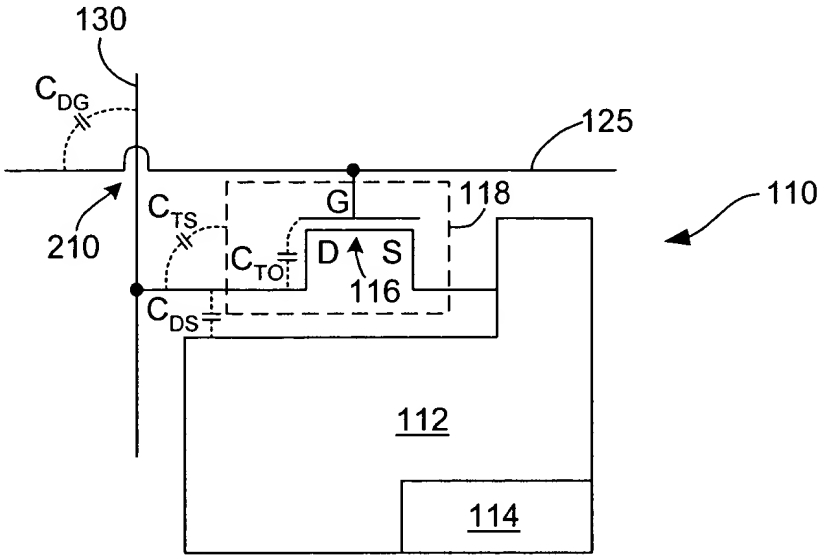

FIG. 2

As explained in Applicants' specification, device performance is related to the signal-to-noise ratio, and a significant source of electronic noise is data line capacitance. Further, Applicants' specification explains that cross-over capacitance C_{DG} is one of the main sources of data line capacitance, particularly in high fill factor devices.

According to the present invention, sensor array 100 is modified to reduce data line capacitance by providing a bridge structure formed at each data line/gate line (metal) crossover 210 (shown in Fig. 2) that reduces the crossover capacitance C_{DG} in comparison with conventional solid dielectric crossover structures by providing a vacuum or gas-filled space (referred to herein as an "air-gap") between the data and gate lines at each crossover 210. In

combination with various optional design techniques, some previously proposed, the air-gap crossover structure of the present invention produces a sensor array exhibiting greatly reduced data line capacitance.

Fig. 3 (reproduced in part below) is a simplified perspective view showing data line 130 forming a bridge structure at crossover location 210 that defines an air-gap 302 extending between a top surface of gate line 125 and a bottom surface of data line 130. Optional spaced-apart support pads 304 are located on opposite sides of air-gap 302 to support and maintain the position of data line 130 relative to gate line 125. Data line 130 is connected by a lateral portion 306 and a via 308 to access transistor 116, which is connected between data line 130 and the sensor structure (omitted in the reproduced Fig. 3 below).

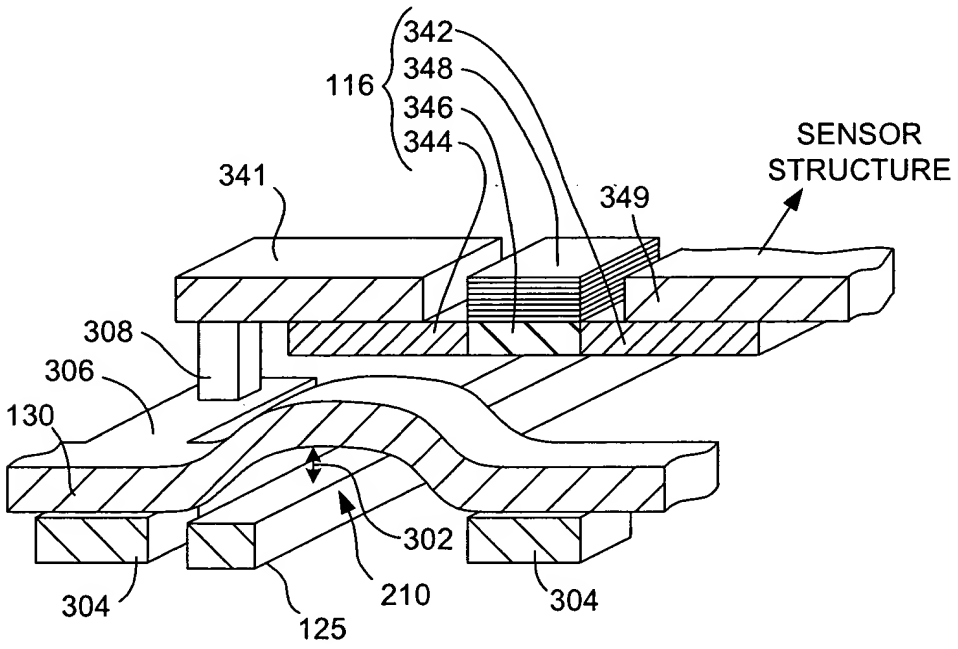

FIG. 3 (PORTIONS REMOVED)

According to another aspect of the present invention, the air-gap structure 302 shown in Fig. 3 is generated using the method illustrated in Applicants' Figs. 4(A) through 4(E), which are reproduced below for reference. In particular, gate line 125 (and optional support structures 334) is formed on an upper surface of a substrate 400 (Fig. 4(A), then a sacrificial (release) material layer 410 is patterned over gate line 125 with optional support structures 334 (or portions of substrate 400) exposed (Fig. 4(B)). Data line 125 is then formed on sacrificial material layer 410 over gate line 125 (Fig. 4(C)), and then the sacrificial material layer 410 is removed (e.g., using a suitable etchant 430 that does not damage data line 130 or gate line 125). Finally, an optional strengthening insulator 440 is formed on data lines 130 at the crossover locations 210 (Fig. 4(E)). Access transistor 116 and the sensor structure are subsequently formed using techniques described in Applicants' specification.

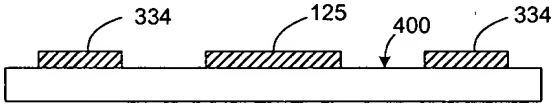

FIG. 4(A)

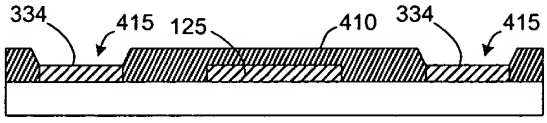

FIG. 4(B)

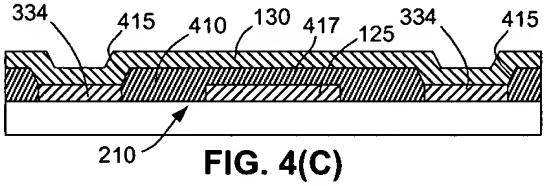

FIG. 4(C)

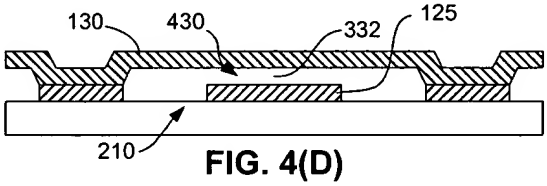

FIG. 4(D)

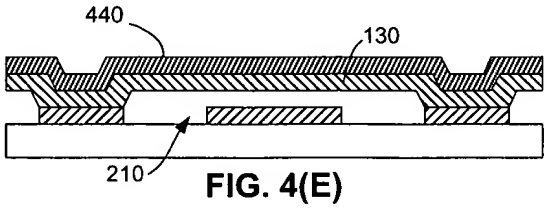

FIG. 4(E)

VI. ISSUES

The following issue is presented to the Board of Appeals for decision:

(A) Whether Claims 1-3 and 6 are unpatentable under 35 U.S.C. 103(a) over Kingsley et al, (USPAT 5587591; herein "Kingsley") in view of Ahn (USPAT 6037248, herein "Ahn");

(B) Whether Claim 4 is unpatentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn, and further in view of Akiyama (USP 5,712,494, herein "Akiyama");

(C) Whether Claim 5 is unpatentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn, and further in view of Hwang (USP 6,337,284, herein "Hwang");

(D) Whether Claim 7 is unpatentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn, and further in view of Street (USP 5,789,737, herein "Street");

(E) Whether Claims 8 and 27-30 are unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn;

(F) Whether Claim 9 is unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn, and further in view of Antonuk (USP 5,262,649, herein "Antonuk");

(G) Whether Claim 10 is unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn, and further in view of Kunikiyo (USPAT 2002/0135041, herein "Kunikiyo");

(H) Whether Claim 21 is unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn, and further in view of Akiyama;

(I) Whether Claim 24 is unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn, and further in view of Hwang;

(J) Whether Claim 25 is unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn and Hwang, and further in view of Pedder (USP 5,604,658, herein "Pedder"); and

(K) Whether Claim 26 is unpatentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn and Hwang, and further in view of Kingsley.

VII. GROUPING OF THE CLAIMS

Claims 1-7 stand or fall together as Group 1.

Claims 8-10 and 21 and 24-30 stand or fall together as Group 2.

VIII. ARGUMENTS

A. Claims 1-3 and 6 are patentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn

Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kingsley et al, (USPAT 5587591; herein "Kingsley") in view of Ahn (USPAT 6037248).

1. The rejection of Claim 1 as unpatentable over Kingsley and Ahn is improper.

Claim 1 recites (in pertinent part) "...an air-gap is defined at each crossover location that separates each first line from the plurality of second lines, wherein each air-gap extends from a top surface of a corresponding second line to a bottom surface of said each first line."

In rejecting Claim 1, the Examiner argues:

> With regard to claim 1, Kingsley discloses in figures 1b – 2b an integrated circuit. Kingsley discloses in figures 1b – 2b a plurality of pixel circuits (134) arranged in rows and columns. Kingsley discloses in figures 1b – 2b a plurality of first lines (132), each first line connected to a corresponding column of pixel circuits. Kingsley discloses in figures 1b – 2b a plurality of second lines (131), each second line connected to a corresponding row of pixel circuits. Kingsley discloses in figure 2b wherein the plurality of first lines are formed such that each first line extends over the plurality of second lines at corresponding crossover locations. Kingsley discloses in figure 2a where an insulator is defined at each crossover location that separates each first line from the plurality of second lines. Kingsley does not disclose that the insulator is an air-gap. Ahn teaches in figure 10 wherein an air-gap (56) is defined at each crossover location that separates a first line (70) from a plurality of second lines (36), wherein each air gap extends from a top surface of a corresponding second line to a bottom surface of the each first line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Kingsley in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

Applicants contend that the above-quoted rejection fails to establish a prima facie case of obviousness under MPEP 706.02(j) at least because it fails to explain why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification (see underlined sections above). Further, as set forth below, the rejection is traversed because (a) neither Kingsley nor Ahn teach or suggest the proposed combiantion, and (b) there is no reasonable expectation that the proposed combination would be successful.

(a) Neither Kingsley nor Ahn teach or suggestion a motivation for the proposed combination

Kingsley teaches a low noise fluoroscopic radiation imager in which a TFT 134 is provided to access an array of photosensors 120. Kingsley teaches that photosensors 120 are arranged with a pitch of 35 to 500 microns, and indicates that the wiring (e.g., scan lines 131 and data lines 132) are located along the periphery of each photosensor "pixel".

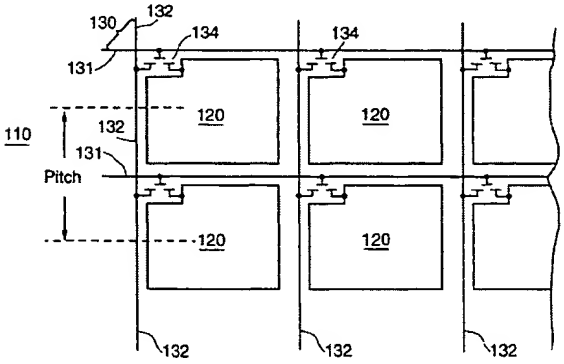

FIG. 1 (B)

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The pitch of imager **100** is determined by the distance between the centers of pixels along a selected axis of the array (e.g., the axis of the data lines **132** as shown in FIG. **1**(B)). Low noise solid state radiation imagers in accordance with this invention typically have a pitch in the

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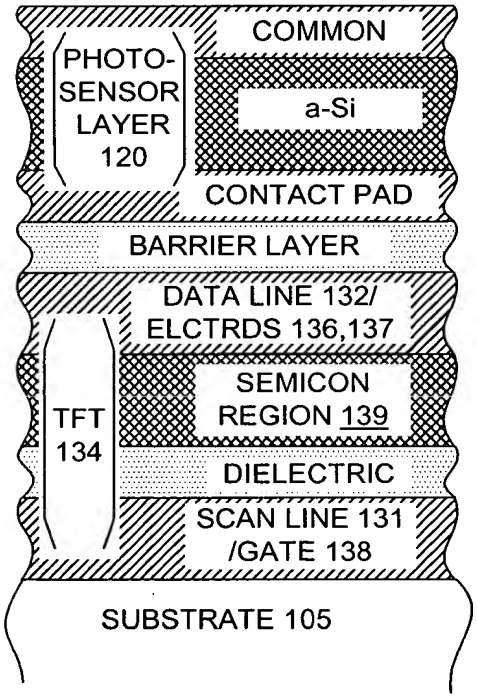
range between about 35 and 500 microns. Imagers having larger areas of switched silicon exhibit higher noise than imagers having smaller areas of switched silicon; higher noise in the imager requires the use of larger x-ray exposures to obtain the same resolution image.

Further, as set forth in the text provided in Kingsley's column 4, line 57 to column 5, line 21 (reproduced below along with a representative cross-section generated by Applicant for reference), Kingsley teaches that the TFT structure is formed under photosensor 120. In

particular, Kingsley teaches forming an array of TFTs by forming scan lines 131 and associated gate electrodes 138 on a substrate 105 using a first metal layer, then forming semiconductor gate structures 139 (amorphous silicon) along with a suitable dielectric layer over corresponding scan lines/gate structures, and then forming data lines 132 and corresponding source electrodes 137 using a second metal layer. As highlighted in the text below, Kingsley points out on line 10 of column 5 that a portion of the dielectric layer is located between the scan and data lines at the "crossovers". Kingsley then teaches forming a dielectric barrier layer over the TFT structures, and then forming photosensors 120 on top of the dielectric layer:



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A representative portion of an imager array **130** comprising a low noise addressable TFT array in accordance with this invention is illustrated in the modified plan view of FIG. 2(A). Components in multiple layers (that is, some components illustrated overlie other components illustrated in this Figure) make up the low noise TFT array. Scan line **131** is typically disposed on substrate **105**; and extension from scan line **131** comprises gate electrode **138** of TFT **134**. A semiconductive region **139** is disposed over gate electrode **134** (with a dielectric layer (not shown), such as silicon nitride or silicon dioxide disposed therebetween). Semicon-

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ductive region typically comprises a layer of amorphous silicon (a-Si) and an overlying layer of doped a-Si (such as a-Si doped to exhibit n type conductivity),

Next, the conductive material comprising data lines **132**, source electrode **137**, and drain electrode **136** are disposed to overly semiconductive region **139**. The conductive material typically comprises chromium, aluminum, molybdenum, tungsten, titanium, and the like. Data line **132** similarly overlies scan line **131** at crossover region **140**, with at least a dielectric material disposed therebetween (typically the same dielectric material disposed between gate electrode **138** and semiconductive region **139**. A barrier layer (not shown) of dielectric material (such as inorganic dielectric material (silicon nitride or the like) and/or organic dielectric material (such as polyimide) is typically disposed over TFT **134** prior to the formation of photosensor **120**; photosensor **120** comprises a bottom electrical contact pad (shown in outline in FIG. 2(A) but not to scale) electrically coupled to source electrode **137**, an overlying photodiode body (not shown) comprising semiconductive layers (e.g., a-Si and doped silicon layers) and a common electrode (not shown) disposed over the top of the photodiode body.

Based on the summarized disclosure above, Applicants contend that Kingsley neither teaches nor suggests replacing the dielectric material located at crossover regions 140 with the "air-gap" arrangement recited in Applicants' Claim 1. Applicant concedes that Kingsley discusses omitting or removing "semiconductive material" from the crossover regions to provide low charge retention structures (see for example, column 6, lines 50-60), but to argue this suggests generating an air gap takes Kingsley completely out of context. That is, Kingsley does not teach or suggest omitting or removing the dielectric material from between the data and scan lines, which would be necessary to produce "air-gap" arrangement recited in Applicants' Claim 1.

Ahn discloses method of fabricating integrated circuit wiring with low RC time delay with reference to the fabrication of a standard MOSFET-type integrated circuit structure. Those of ordinary skill in the art will recognize the MOSFET-type structure disclosed in Ahn's Fig. 2 and associated description (reproduced below for reference) includes a polysilicon gate structure 36 formed on a gate oxide 33, and diffusion areas 38 formed on either side of the gate structure:

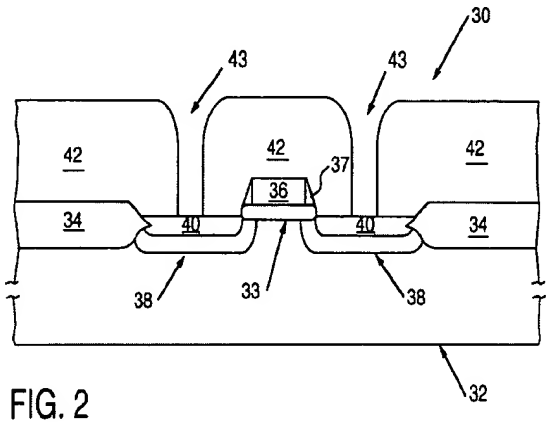

FIG. 2

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FIG. 2 shows a cross-section of a substrate assembly **30** at an early stage in the fabrication process of the present invention. The substrate assembly **30** includes a substrate layer **32**, which is the lowest layer of semiconductor material on a wafer, and additional layers or structures formed thereon. A LOCOS process is performed to provide a layer of gate oxide **33** separated by field oxide regions **34**. A polysilicon layer **36** is deposited and etched to provide a contact area, typically for the gate terminal of a transistor. A spacer **37** may be formed along the layer **36** using conventional techniques. Impurities are diffused into the substrate **34** through suitable masks to form diffusion areas **38**. The diffusion areas **38** give rise to depletion regions that essentially isolate the source and drain terminals of the transistor from one another by two diodes. Silicide layers **40** are formed on the diffusion areas **38**. The silicide layers **40** are formed by depositing a refractory metal such as titanium, platinum, palladium, cobalt, or tungsten on polysilicon. The metal/silicon alloy is then sintered to form the silicide layers **40**.

Above the basic MOSFET-type structure introduced in

Ahn's Fig. 2, Ahn discloses forming alternate layers of photoresist and metal, patterning the metal to form columns, and then removing the photoresist by ashing to form metal layers that are supported on the columns, thereby providing a completed integrated circuit structure in which the metal layers are separated from the underlying circuit structure by air gaps 56:

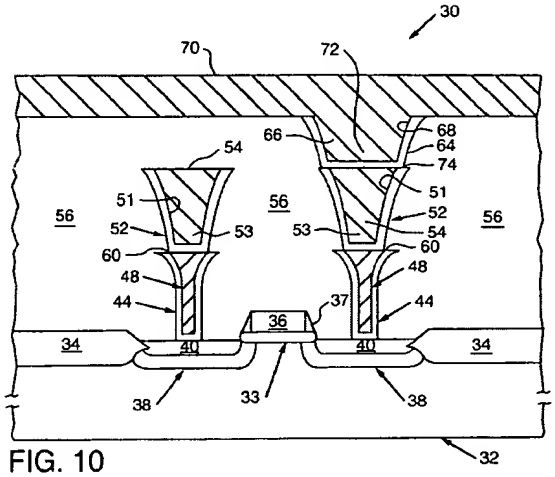

FIG. 10

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FIG. 10 shows a resulting substrate assembly 30 of FIG. 9 with the first metal layer 54 and the second metal layer 70 formed. The photoresist layers 42, 50 and 62 are removed by, for example, ashing in oxygen plasma to form air gaps 56. The metal layers 54 and 70 are supported by columns 60 and 74 formed by the combination of the metal plugs 48 and 66 and the contacts 53 and 72. The air gaps 56 have a dielectric constant of 1, thereby reducing the capacitance of the resulting structure. By selecting appropriate metal conductors which have a low resistance, the RC time constant of the resulting structure is reduced.

Applicants contend that Ahn neither teaches nor suggests that the disclosed air gap structure could be utilized to modify the fluoroscopic radiation imager of Kingsley. That is, as set forth above, the fabrication method taught by Ahn involves the formation of metal columns to separate the metal layers from the underlying substrate/circuitry. Ahn neither teaches nor suggests that the disclosed column struture could be modified such that it would be suitable to provide air gaps between the data lines and scan lines of Kingsley's fluoroscopic radiation imager.

(b) There is no reasonable expectation that the combination of Kingsley and Ahn would be successful

MPEP section 2143 reads (in relevant part):

AT LEAST SOME DEGREE OF PREDICTABILITY IS REQUIRED; APPLICANTS MAY PRESENT EVIDENCE SHOWING THERE WAS NO REASONABLE EXPECTATION OF SUCCESS

Obviousness does not require absolute predictability, however, at least some degree of predictability is required. Evidence showing there was no reasonable expectation of success may support a conclusion of nonobviousness. *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) (Claims directed to a method for the commercial scale production of polyesters in the presence of a solvent at superatmospheric pressure were rejected as obvious over a reference which taught the claimed method at atmospheric pressure in view of a reference which taught the claimed process except for the presence of a solvent. The court reversed, finding there was no reasonable expectation that a process combining the prior art steps could be successfully scaled up in view of unchallenged evidence showing that the prior art processes individually could not be commercially scaled up successfully.). See also *Amgen, Inc. v. Chugai Pharmaceutical Co.*, 927 F.2d 1200, 1207-08, 18 USPQ2d 1016, 1022-23 (Fed. Cir.), *cert. denied*, 502 U.S. 856 (1991) (In the context of a biotechnology case, testimony supported the conclusion that the references did not show that there was a reasonable expectation of success.); *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (The court held the claimed method would have been obvious over the prior art relied upon because one reference contained a detailed enabling methodology, a suggestion to modify the prior art to produce the claimed invention, and evidence suggesting the modification would be successful.).

Applicants presented arguments in the last submitted paper that the combination proposed by the Examiner would not produce a suitable structure. These arguments are repeated below.

First, utilizing the teachings of Ahn would require replacing Kingsley's dielectric layer with photoresist. That is, in order to form the "air gap crossover" taught by Ahn, the dielectric layer located between Kingsley's scan lines 131 and data lines 132 at the "crossovers" must be replaced with photoresist that can be subjected to the ashing process described by Ahn. However, as set forth above, Kingsley teaches that this dielectric is also located between gate structures 139 and corresponding scan lines 131/gate structures 138. Accordingly, removing the photoresist from between scan lines 131 and data lines 132, as taught by Ahn, would also damage the TFT structure by undercutting semiconductor region 139, possibly causing contact between semiconductor 139 and scan line 131.

Accordingly, it would not have been obvious to modify Kingsley using the method taught by Ahn because the resulting structure could be inoperable.

Second, the structure taught by Ahn would fail to provide proper support for the photosensor structure utilized in Kingsley. As set forth above, the data wires utilized by Kingsley are spaced at a pitch of 35 to 500 microns. Removing dielectric/photoresist from between these widely spaced wires would produce voids (holes) that would greatly complicate the subsequent formation of Kingsley's overlying photosensor. That is, the scan lines 131 and data lines 132 taught by Kingsley are located below photosensor layer 120 (see diagram on page 12 of this paper), whereas Ahn's metal layers form the upper portion of the fabricated circuit structure (i.e., Ahn's metal layers do not support, for example, a photosensor structure). Due to the wide spacing between scan lines 131 and data lines 132, producing the structure of Kingsley using the air gap arrangement of Ahn would provide little or no support for the subsequently formed photosensor. Accordingly, it would not have been obvious to modify Kingsley using the method taught by Ahn because the resulting structure would be substantially more difficult to produce and/or inoperable.

For at least the above reasons, Applicants contend that the rejection of Claim 1 is improper and should be withdrawn. In particular, not only does the rejection of Claim 1 fail to properly identify a motivation for combining the Ahn and Kingsley, Applicants have shown that such a motivation does not exist. Further, Applicants have pointed out that modifying Kingsley to include the air gap structures taught by Ahn would likely produce an inoperable structure. Accordingly, Applicants respectfully request

that the rejection of Claim 1 be removed and Claim 1 passed to issuance.

2. The rejections of Claims 2, 3 and 6 as unpatentable over Kingsley and Ahn are improper for at least the reasons provided with reference to Claim 1.

Claims 2, 3 and 6 are dependent from Claim 1, and are therefore believed to be patentable over Kingsley and Ahn for at least the same reasons as those set forth with respect to Claim 1.

B. Claim 4 is patentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn and Akiyama

Claim 4 is rejected under 35 USC 103 as being unpatentable over Kingsley in view of Ahn, and further in view of Akiyama.

Claim 4 is dependent from Claim 1, and is therefore believed to be patentable over Kingsley and Ahn for at least the same reasons as those set forth above with respect to Claim 1. Further, Akiyama fails to overcome the deficiencies of Kingsley and Ahn (discussed above) with respect to the structures recited in Claim 1. Therefore, Claim 4 is believed to be patentable for reasons similar to those set forth above with respect to Claim 1.

C. Claim 5 is patentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn and Hwang

Claim 5 is rejected under 35 USC 103 as being unpatentable over Kingsley in view of Ahn, and further in view of Hwang.

Claim 5 is dependent from Claim 1, and is therefore believed to be patentable over Kingsley and Ahn for at least the same reasons as those set forth above with respect to Claim 1. Further, Hwang fails to overcome the deficiencies of Kingsley and Ahn (discussed above) with respect to the

structures recited in Claim 1. Therefore, Claim 5 is believed to be patentable for reasons similar to those set forth above with respect to Claim 1.

D. Claim 7 is patentable under 35 U.S.C. 103(a) over Kingsley in view of Ahn and Street

Claim 7 is rejected under 35 USC 103 as being unpatentable over Kingsley in view of Ahn, and further in view of Street.

Claim 7 is dependent from Claim 1, and is therefore believed to be patentable over Kingsley and Ahn for at least the same reasons as those set forth above with respect to Claim 1. Further, Street fails to overcome the deficiencies of Kingsley and Ahn (discussed above) with respect to the structures recited in Claim 1. Therefore, Claim 7 is believed to be patentable for reasons similar to those set forth above with respect to Claim 1.

E. Claims 8 and 27-30 are patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn

Claims 8 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda et al, (USPAT 5623161; herein "Fukuda") in view of Ahn.

1. The rejection of Independent Claim 8 as unpatentable over Fukuda and Ahn is improper.

Similar to Claim 1, independent Claim 8 recites (in pertinent part) "...an air-gap is defined at each crossover location that separates each data line from the plurality of gate lines such that each air-gap extends from a top surface of a corresponding gate line to a bottom surface of said each data line."

In rejecting Claim 8, the Examiner writes:

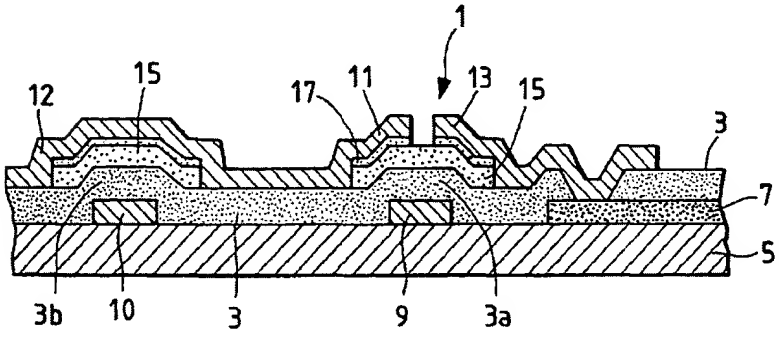
> With regard to claim 8, Fukuda discloses in figures 1 and 2 an image sensor array. Fukuda discloses in figures 1 and 2 and column 4, lines 57 – 67 a plurality of pixel circuits arranged in rows and columns, each pixel circuit including an access transistor (1). Fukuda discloses in figures 1 and 2 a plurality of gate lines (10), each gate line connected (9) to the access transistors of a corresponding column of pixel circuits. Fukuda discloses in figures 1 and 2 a plurality of data lines (12), each data line connected (11) to the access transistors of a corresponding row of pixel circuits. Fukuda discloses in figures 1 and 2 wherein the plurality of data lines are formed such that each data line overlaps the plurality of gate lines at corresponding crossover locations. Fukuda discloses in figures 1 and 2 where an insulator (3) is defined at each crossover location that separates each data line from the plurality of gate lines. Fukuda does not disclose that the insulator is an air-gap. Ahn teaches in figure 10 wherein an air-gap (56) is defined at each crossover location that separates a data line (70) from the plurality of gate lines (36), wherein each air gap extends from a top surface of a corresponding gate line to a bottom surface of the each data line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Fukuda in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

Applicants again contend that the above-quoted rejection fails to establish a prima facie case of obviousness under MPEP 706.02(j) at least because it fails to explain why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification. Further, as set forth in the following paragraphs, the rejection is traversed because (a) neither Fukada nor Ahn teach or suggest the proposed combination, and (b) there is no reasonable expectation that the proposed combination would be successful.

(a) Neither Fukada nor Ahn teach or suggestion a motivation for the proposed combination

Referring to Fukuda's Fig. 8 (reproduced below), Fukada teaches an electronic element including a gate electrode 9 and a gate wire 10 formed on a substrate 5, an insulating film 3 including a gate insulating filmm 3a and an interlayer insulating film 3b, source electrode 11, a source wire 12, and a drain electrode 13. Fukuda teaches that silicon nitride is frequently used as insulating film 3, but that such a practice may result in a sotrt circuit between gate electrode 9/wire 10 and source electrode 11/wire 12:

FIG. 8 PRIOR ART



1

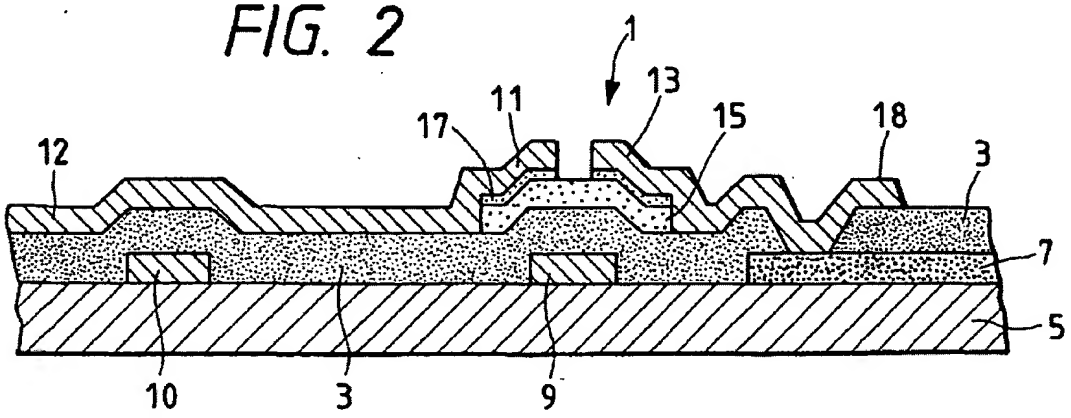
However, in any electronic element represented by a TFT where such a silicon nitride insulating film is used as the gate insulating film 3*a* or the interlayer insulating film 3*b* at the intersection of multilayer wires, there may arise a problem of electric short circuit among the gate electrode 9, the gate wire 10 and the wire (source wire 12, source electrode 11 or the like) formed via an insulating film. Particularly on any substrate having a high integration density or a large area, the probability of such short-circuiting trouble is rendered extremely high.

Fukuda addresses the established "shorting" problem by teaching the use of a silicon nitride film having an oxygen content that is less than 10 atomic percent:

According to one aspect of the present invention, there is provided an electronic element where a conductive wire pattern is formed on the surface of a substrate which is insulative at least in its surface, and an insulating layer is formed on the substrate and the wire pattern in a manner to cover the same either partially or entirely. In this electronic element, the insulating layer is composed of such a silicon nitride film that, at least in the vicinity of a step portion of the pattern, the oxygen content is less than 10 atomic percent.

Moreover, Fukuda neither teaches nor suggests omitting the silicon nitride insulating layer 3, and clearly discloses the presence of insulating layer 3 between gate wire 10 and source wire 12 at each intersection:

FIG. 2



Based on the summarized disclosure above, Applicants contend that Fukuda neither teaches nor suggests replacing the silicon nitride insulating layer with the "air-gap" arrangement recited in Applicants' Claim 1.

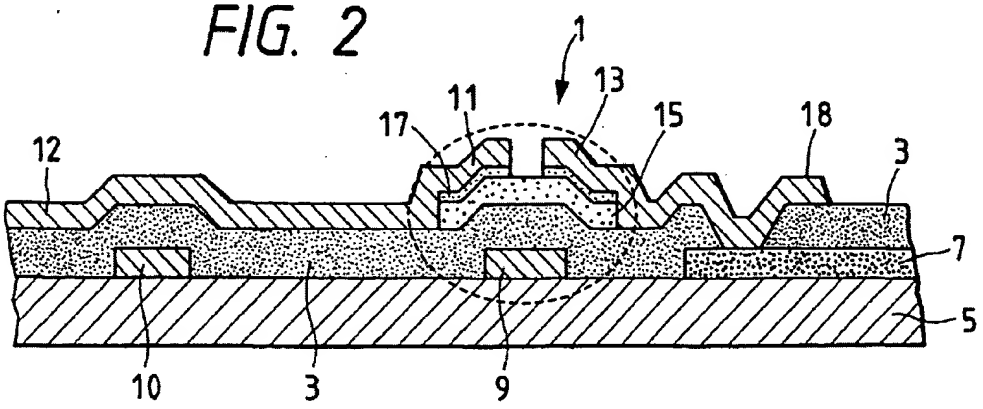
Ahn is discussed above. For reasons similar to those provided above with reference to Kingsley, Applicants contend that Ahn fails to teach our suggest a motivation for utilizing Ahn's air gap structure to modify the circuit arrangement taught by Fukuda. That is, as set forth above, the fabrication method taught by Ahn involves the formation of metal columns to separate the metal layers from the underlying substrate/circuitry. Ahn neither teaches nor suggests that the disclosed column structure could be

modified such that it would be suitable to provide air gaps between the gate and source lines of Fukuda.

(b) There is no reasonable expectation that the combination of Fukuda and Ahn would be successful

Similar to the arguments raised above with respect to Kingsley, Applicants contend that the combination proposed by the Examiner in rejecting Claim 8 would not produce a suitable structure. In particular, utilizing the teachings of Ahn would require replacing Fukuda's silicon nitride insulating layer 3 both beneath the intersection of gate line 10 and source line 12, and also in the channel region between gate electrode 9 and amorphous silicon gate structure 15, which would cause silicon gate structure 15 to collapse (Applicants point out that Ahn does not teach supporting amorphous silicon gate structures).

FIG. 2



Accordingly, it would not have been obvious to modify Fukuda using the method taught by Ahn because the resulting structure could be inoperable.

For at least the above reasons, Applicants contend that the rejection of Claim 8 is improper and should be withdrawn. In particular, not only does the rejection of Claim 8 fail to properly identify a motivation for combining the air gap structure of Ahn with the structure of Fukuda,

Applicants have shown that such a motivation does not exist. Further, Applicants have pointed out that modifying Fukuda to include the air gap structures taught by Ahn would likely produce an inoperable structure. Accordingly, Applicants respectfully request that the rejection of Claim 8 be removed and Claim 8 passed to issuance.

2. The rejections of Independent Claims 28 and 30 as unpatentable over Fukuda and Ahn are improper for at least the reasons discussed above with reference to Claim 8.

Independent Claims 28 and 30 are rejected for reasons similar to those used to reject Claim 8. In particular, in rejecting Claim 28, the Examiner identifies corresponding structures associated with Fukuda, and then writes:

> ... Fukuda is silent to air gaps. Ahn teaches in figure 10 second portions extending over a plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Fukuda in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

Similarly, in rejecting Claim 30, the Examiner writes:

> ... Fukuda is silent to air gaps. Ahn teaches in figure 10 second portions extending between adjacent first portions such that each second portion is freely supported by an associated pair of adjacent first portions, wherein each second portion extends over a corresponding first line such that an air gap is defined between the corresponding first line and said each second portion, over a plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Fukuda in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

For at least the reasons provided above with reference to the rejection of Claim 8, Applicants believe the above-quoted rejections directed to Claims 28 and 30 are improper, and should be withdrawn. In particular, not only do these rejections fail to properly identify a motivation for combining the air gap structure of Ahn with the structure of Fukuda, Applicants have shown that such a motivation does not exist. Further, Applicants have pointed out that modifying Fukuda to include the air gap structures taught by Ahn would likely produce an inoperable structure. Accordingly, Applicants respectfully request that the rejections of independent Claims 28 and 30 be removed, and that Claims 28 and 30 be passed to issuance.

3. The rejections of Claims 27 and 29 as unpatentable over Fukuda and Ahn are improper for at least the reasons discussed above with reference to Claims 8 and 28.

Claim 27 is dependent from Claim 8, and Claim 29 is dependent from Claim 28. Therefore, both of these claims believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth with respect to Claims 8 and 28.

F. Claim 9 is patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn and Antonuk

Claim 9 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Ahn, and further in view of Antonuk.

Claim 9 is dependent from Claim 8, and is therefore believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth above with respect to Claim 8. Further, Antonuk fails to overcome the deficiencies of Fukuda and Ahn (discussed above) with respect to the structures recited in Claim 8. Therefore, Claim 9 is

believed to be patentable for reasons similar to those set forth above with respect to Claim 8.

G. Claim 10 is patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn and Kunikiyo

Claim 10 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Ahn, and further in view of Kunikiyo.

Claim 10 is dependent from Claim 8, and is therefore believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth above with respect to Claim 8. Further, Kunikiyo fails to overcome the deficiencies of Fukuda and Ahn (discussed above) with respect to the structures recited in Claim 8. Therefore, Claim 10 is believed to be patentable for reasons similar to those set forth above with respect to Claim 8.

H. Claim 21 is patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn and Akiyama, and Claims 22 and 23 should be reinstated X

Claim 21 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Ahn, and further in view of Akiyama.

Claim 21 is dependent from Claim 8, and is therefore believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth above with respect to Claim 8. Further, Akiyama fails to overcome the deficiencies of Fukuda and Ahn (discussed above) with respect to the structures recited in Claim 8. Therefore, Claim 21 is believed to be patentable for reasons similar to those set forth above with respect to Claim 8.

Because Claim 21 is allowable, Applicants respectfully request reinstatement of Claims 22 and 23, which were withdrawn by the Examiner.

I. Claim 24 is patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn and Hwang

Claim 24 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Ahn, and further in view of Hwang.

Claim 24 is dependent from Claim 8, and is therefore believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth above with respect to Claim 8. Further, Hwang fails to overcome the deficiencies of Fukuda and Ahn (discussed above) with respect to the structures recited in Claim 8. Therefore, Claim 24 is believed to be patentable for reasons similar to those set forth above with respect to Claim 8.

J. Claim 25 is patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn, Hwang and Pedder

Claim 25 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Ahn, and further in view of Hwang and Pedder.

Claim 25 is ultimately dependent from Claim 8, and is therefore believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth above with respect to Claim 8. Further, Hwang and Pedder fail to overcome the deficiencies of Fukuda and Ahn (discussed above) with respect to the structures recited in Claim 8. Therefore, Claim 25 is believed to be patentable for reasons similar to those set forth above with respect to Claim 8.

K. Claim 26 is patentable under 35 U.S.C. 103(a) over Fukuda in view of Ahn, Hwang and Kingsley

Claim 26 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Ahn, and further in view of Hwang and Kingsley.

Claim 26 is ultimately dependent from Claim 8, and is therefore believed to be patentable over Fukuda and Ahn for at least the same reasons as those set forth above with respect to Claim 8. Further, Hwang and Kingsley fail to overcome the deficiencies of Fukuda and Ahn (discussed above) with respect to the structures recited in Claim 8. Therefore, Claim 26 is believed to be patentable for reasons similar to those set forth above with respect to Claim 8.

IX. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 1-10 and 21 and 24-30 are erroneous, and reversal of these rejections is respectfully requested. It is also submitted that, due to the allowability of Claim 21, Claims 22 and 23 should be reinstated and passed to issuance.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Services as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450.

Attorney for Appellant

Oct 1, 2003
Date of Signature

X. APPENDIX A

1. (Amended) An integrated circuit comprising:

a plurality of pixel circuits arranged in rows and columns;

a plurality of first lines, each first line connected to a corresponding column of pixel circuits; and

a plurality of second lines, each second line connected to a corresponding row of pixel circuits,

wherein the plurality of first lines are formed such that each first line extends over the plurality of second lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each first line from the plurality of second lines, wherein each air-gap extends from a top surface of a corresponding second line to a bottom surface of said each first line.

2. (Amended) The integrated circuit according to Claim 1, wherein each pixel circuit includes an access transistor and a pixel element, wherein the access transistor includes a gate terminal connected to an associated first line, a first terminal connected to the pixel element, and a second terminal connected to an associated second line.

3. (Original) The integrated circuit according to Claim 2, wherein the access transistor comprises one of amorphous silicon and polysilicon.

4. (Original) The integrated circuit according to Claim 2, wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor.

5. (Original) The integrated circuit according to

Claim 2, wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated second line by a buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

6. (Original) The integrated circuit according to Claim 2, wherein the integrated circuit comprises a medical image sensor array.

7. (Original) The integrated circuit according to Claim 2, wherein each pixel element comprises an amorphous silicon sensor, and each pixel circuit further comprises a phosphor converter located over the amorphous silicon sensor.

8. (Amended) An image sensor array comprising:

a plurality of pixel circuits arranged in rows and columns, each pixel circuit including an access transistor;

a plurality of gate lines, each gate line connected to the access transistors of a corresponding column of pixel circuits; and

a plurality of data lines, each data line connected to the access transistors of a corresponding row of pixel circuits,

wherein the plurality of data lines are formed such that each data line overlaps the plurality of gate lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each data line from the plurality of gate lines such that each air-gap extends from a top surface of a corresponding gate line to a bottom surface of said each data line.

9. (Original) The image sensor array according to Claim 8,

wherein the plurality of gate lines are formed from a first metal layer, the plurality of data lines are formed from a second metal layer such that the data lines are located above the first metal layer, wherein each of the plurality of pixel circuits also comprises a sensor including an amorphous silicon (a-Si:H) layer formed on a metal plate, and

wherein the metal plate is formed from a third metal layer formed after the first and second metal layers.

10. (Original) The image sensor array according to Claim 8, further comprising a strengthening insulator formed on the plurality of data lines at the crossover locations.

21. (As entered) The image sensor array according to Claim 8, wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor.

22. (Withdrawn) The image sensor array according to Claim 21, wherein the self-aligned thin-film transistor of each pixel circuit comprises:

an amorphous silicon (a-Si:H) layer including a relatively undoped first region located over an associated gate line, the first region being located between a doped second region and a doped third region; and

an optical filter island located over the first region, the optical filter island comprising at least three layers having at least two indexes of refraction and being arranged such that the optical filter island is reflective of a first radiation wavelength and transmissive of a second radiation wavelength.

23. (Withdrawn) The image sensor array according to Claim 22,

wherein each of the plurality of pixel circuits also comprises a sensor including an amorphous silicon (a-Si:H) layer formed on a metal plate,

wherein the metal plate is connected to the doped second region of the self-aligned thin-film transistor, and

wherein an associated data line is connected to the doped third region of the self-aligned thin-film transistor.

24. (As entered) The image sensor array according to Claim 8, wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated data line by a buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

25. (As entered) The image sensor array according to Claim 24, wherein the buried insulator layer has a thickness of 3 to 5 microns.

26. (As entered) The image sensor array according to Claim 24, wherein the charge sensing region of each of the plurality of pixel circuits comprises an amorphous silicon (a-Si:H) layer.

27. (Amended) The image sensor array according to Claim 8,

wherein the image sensor array further comprises spaced-apart data line support pads, and

wherein each spaced-apart data line support pad contacts an associated data line.

28. (As entered) An image sensor array comprising:

a substrate having an upper surface defining a plane;

a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate;

a plurality of first lines, each first line being formed on the upper surface of the substrate and connected to a corresponding first group of said pixel circuits; and

a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:

first portions supported by the upper surface of the substrate, and

second portions extending over the plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line.

29. (As entered) The image sensor array according to Claim 28, further comprising a plurality of support pads, each support pad being formed on the upper surface of the substrate and contacting a corresponding first portion of an associated second line.

30. (As entered) An image sensor array comprising:

a substrate having an upper surface defining a plane;

a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate;

a plurality of first lines, each first line being formed over the upper surface of the substrate and connected to a corresponding first group of said pixel circuits;

a plurality of support pads, each support pad being

formed over the upper surface of the substrate; and

a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:

a plurality of first portions, each first portion contacting a corresponding support pad, and

second portions extending between adjacent first portions such that each second portion is freely supported by an associated pair of adjacent first portions, wherein each second portion extends over a corresponding first line such that an air gap is defined between the corresponding first line and said each second portion.